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09/975,630	10/12/2001	Taylor R. Efland	TI-31678	8387

7590 05/21/2003

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EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/975,630	Applicant(s) EFLAND, TAYLOR R.
	Examiner Leonardo Andújar	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-23* is/are pending in the application.

4a) Of the above claim(s) *20-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *03 March 2003* is: a)☐ approved b)☒ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4)☐ Interview Summary (PTO-413) Paper No(s). _____
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other:

DETAILED ACTION

Acknowledgment

1. The amendment filed on 03/03/03, paper no. 6, in response to the Office action mailed on 10/24/2002 has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1-3 and 5-20.

Election/Restrictions

2. Applicant's election without traverse of Group I in Paper No. 3 is acknowledged.

Drawings

3. The proposed drawing correction filed on 03/03/2003 has been disapproved because the drawings do not show every feature of the invention specified in the claims. For example, the encapsulation according to claim 8, the lead frame segment portions not included in the encapsulation according to claim 10 and the solder balls attached to the electrical conductor connecting the network lines to the second plurality of segments according to claim 11.

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the stress absorbing film(s), the outermost film, chip mount pad, chip contact pads according to claim 2, the multi-layer metallization according to claim 5, the encapsulation according to claim 8, the lead frame segment portions not included in the encapsulation according to claim 10, the solder balls attached to the electrical conductor connecting the network lines to the second plurality of segments according to claim 11 and the solder balls conductors

according to claim 15 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 17 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification does not disclose that the claimed invention includes a solder ball made of pure tin, tin alloys including tin/copper, tin/indium, tin/silver, tin/bismuth, tin/lead, and conductive adhesive compounds according to claim.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Yamasaki et al. (US 5,973,554).

9. Regarding claim 1, Yamasaki (figs. 1-5) shows an integrated circuit chip 71 mounted on a lead frame (61-65) comprising a network distribution lines 5 deposited on the surface of the chip, located directly over active component 70 of the circuit. As shown in figure 5 the lines are conductively and vertically connected to the active components below the lines. Also, the lines are connected to a lead frame 62 by conductors 66 (e.g. fig. 1).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 2-6, 8-10, 12-16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al. (US 5,973,554) in view of Tani (US 5,468,993).

12. Regarding claim 2, Yamasaki discloses a semiconductor device comprising;

- A semiconductor chip having a first and second surface, an active component 70;
- A metal layer 3 protected by a mechanically strong, electrically insulating overcoat 6 having a plurality of metal filled vias 9 to make an electrical contact;
- A plurality of windows to expose the circuit contact pads;
- Electrically conductive films (4, 5) deposited on the overcoat and patterned into a network of lines substantially vertically over the active components, the film is in

contact with the vias 9 and having at least one stress absorbing film 4 and an outermost film 5 being non corrodible and metallurgical attachable.

- A lead frame (61-65) having a first plurality of segments providing electrical signal and a second plurality of providing power and ground;
- Electrical conductors 66 connecting the chip contact pads (P1-P5) and/or the connecting the network lines with the plurality of segments.

13. The network pattern distributes the power current and the ground potential (e.g. fig. 5). Yamasaki discloses that the chip is mounted in the lead frame. Nonetheless, Yamasaki fails to further specify that the semiconductor chip is mounted in a chip mount pad. Tani discloses that it is conventionally in the art to attach the semiconductor chip to a chip mount pad (col. 1/lls. 17-28). As shown in fig. 3 the second surface of the chip 3 is attached to the chip mount pad 1. It would have been obvious to one of ordinary skill in the art at the time the invention was made to attach the second surface of the semiconductor chip to a chip mount pad as it is conventionally in the art as taught by Tani.

14. Regarding claim 3, Yamasaki discloses that the chip is made of silicon (col. 2/lls. 64-66).

15. Regarding claim 5, Yamasaki discloses that the circuit comprises multi-layer metallization made of aluminum (col. 8/lls. 9-51).

16. Regarding claim 6, Yamasaki discloses the claimed invention except for the use of silicon nitride, silicon oxynitride, silicon carbon alloys or polyimide for make the overcoat 6. It would have been obvious to one having ordinary skill in the art at the time

the invention was made to use of silicon nitride, silicon oxynitride, silicon carbon alloys or polyimide for make the overcoat 6, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ416.

17. Regarding claims 8 and 9, Tani discloses that the semiconductor chip and the bonded portion are sealed by synthetic resin molding or molding (col. 1/lls.19-28). Tani does not specify the process used to make the encapsulation e.g. transfer molding process. Nonetheless, this limitation is considered a process limitation. Note that in product related claims only the final product is relevant, not the process of making such as transfer molding. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17. See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

18. Regarding claim 10, Tani discloses that the lead frame segment portions are not included in the encapsulation. Also, the leads are shaped as leads which are solderable to the outside parts (e.g. fig. 3, col. 1/lls.19-28).

19. Regarding claim 12, Yamasaki shows that the conductors/ metallurgical attachments are bonding wires.

20. Regarding claim 13, Yamasaki shows that the stress absorbing metal layer 4 is made of aluminum (col. 8/lls. 9-51).

21. Regarding claim 14, Yamasaki shows that the outermost metal layer 5 is made of aluminum (col. 8/lls. 9-51).

22. Regarding claim 15, Yamasaki shows that the conductors are bonding wires.

23. Regarding claim 16, Tani discloses that the semiconductor chip is bonded to the leads radially disposed around the die pad with gold wires (col. 1/lls.19-28).

24. Regarding claim 18, Yamasaki shows that the network of lines is electrically connected to the segments that are suitable for outside electrical contact.

25. Regarding claim 19, Yamasaki shows that the network of lines, together with the metal filled vias provides a power distribution function to the active components.

26. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al. (US 5,973,554) in view of Tani (US 5,468,993) in view of Applicant's Admitted Prior Art.

27. Regarding claim 7, Yamasaki in view of Tani shows most aspects of the instant invention. Yamasaki in view of Tani does not disclose that the lead frame is made from a material selected from a group consisting of copper, copper alloy, aluminum, iron nickel alloy or invar. However, Applicant's Admitted Prior Art discloses that it has been common practice to manufacture single piece lead frames from thin sheets of metal. For reasons of easy manufacturing, the commonly selected starting metals are copper,

copper alloy, iron nickel alloys and invar (pp. 005). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the lead frame of Yamasaki in view of Tani of copper, copper alloy, iron nickel alloys or invar for easy manufacturing reasons as taught by Applicant's Admitted Prior Art.

28. Claims 11, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al. (US 5,973,554) in view of Tani (US 5,468,993) in view of Wolf et al.

29. Regarding claim 11, Yamasaki in view of Tani shows most aspects of the instant invention including lines and contacts pads attached to the outside part by conductors 66. However, Yamasaki in view of Tani does not disclose that solder balls can be used as connection means. Nonetheless, the use of wire bonds or solder balls as connection means is considered an obvious design choice and it is not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416. For example, the advantages of flip chip bonding (solder ball or C4) are: 1) the entire chip surface can be covered with solder bumps. In other words, bonding locations are not limited to the chip perimeter, thus more I/O capability is provided than by a perimeter interconnections on a die with the same size, and 2) the very short lengths of the chip to package interconnection paths minimizes their inductance (see Wolf pages 857-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use solder balls to make

the electrical connections of the device disclosed by Yamasaki in view of Tani in order to provide more I/O capability and to minimizes the inductance as taught Wolf.

30. Regarding claim 15, Yamasaki in view of Tani shows most aspects of the instant invention including bonding wires conductors. However, Yamasaki in view of Tani does not disclose that solder balls can be used as connection means. Nonetheless, the use of wire bonding or solder ball connections is considered an obvious design choice and it is not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416. For example, the advantages of flip chip bonding (solder ball or C4) are: 1) the entire chip surface can be covered with solder bumps. In other words, bonding locations are not limited to the chip perimeter, thus more I/O capability is provided than by a perimeter interconnections on a die with the same size, and 2) the very short lengths of the chip to package interconnection paths minimizes their inductance (see Wolf pages 857-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use solder balls to make the electrical connections of the device disclosed by Yamasaki in view of Tani in order to provide more I/O capability and to minimizes the inductance as taught Wolf.

31. Regarding claim 17, Wolf discloses that the can be made of tin/lead alloy (pages 857-8).

Response to Arguments

32. Applicant's arguments filed 03/03/2003 have been fully considered but they are not persuasive. Applicant argues that the element 70 in Yamasaki's invention is a passive element. Nonetheless, Yamasaki clearly discloses that the element 70 is an active element (col. 2/ll. 62).

33. Applicant argues that Yamasaki does not disclose a stress absorbing film. Nonetheless, Yamasaki shows a stress absorbing film 4. Although the applicant uses terms different to those of Yamasaki to label the claimed invention, this does not result in any structural difference between the claimed invention and the prior art. Note that the use of different terminology to describe the plurality of elements that constitute an integrated circuit is just a writing style and the way in which a structural limitation is expressed does not affect the configuration of the described elements. Moreover, any material that is capable of being deformed absorbs stress (e.g. aluminum).

34. In response to applicant's argument that Tani is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Tani is in the field of applicant's endeavor (semiconductor packaging). Also, Tani discloses that it is conventionally in the art to attach the semiconductor chip to a chip mount pad (col. 1/lls. 17-28)

Conclusion

35. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

36. Papers related to this application may be submitted directly to Art Unit 2826 by facsimile transmission. Papers should be faxed to Art Unit 2826 via the Art Unit 2826 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2826 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2826 Fax Center is to be used only for papers related to Art Unit 2826 applications.

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Leonardo Andújar** at **(703) 308-0080** and between the hours of 9:00 AM to 7:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Leonardo.Andujar@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn, can be reached on (703) 308-6601.

38. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 305-3900.**

39. The following list is the Examiner's field of search for the present Office Action:

U.S. Class / Subclass (es): 257/207, 208, 209, 691, 666	05/03
Other Documentation:	
Electronic Database(s): East (USPAT, US PGPUB, JPO, EPO, Derwent, IBM TDB)	05/03

Leonardo Andújar
Patent Examiner Art Unit 2826
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5/16/03